

IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL
BARRIER INTERPOLY INSULATORS

Abstract of the Disclosure

5 Structures and methods for in service programmable logic arrays with low
tunnel barrier interpoly insulators are provided. The in-service programmable logic
array includes a first logic and a second logic plan having a number of logic cells
arranged in rows and columns that are interconnected to produce a number of logical
10 outputs such that the in service programmable logic array implements a logical
function. The logic cell includes a first source/drain region and a second
source/drain region separated by a channel region in a substrate. A floating gate
opposing the channel region and is separated therefrom by a gate oxide. A control
gate opposes the floating gate. The control gate is separated from the floating gate
15 by a low tunnel barrier intergate insulator. The low tunnel barrier intergate insulator
includes a metal oxide insulator selected from the group consisting of PbO, Al₂O₃,
Ta₂O₅, TiO₂, ZrO₂, Nb₂O₅ and/or a Perovskite oxide tunnel barrier.

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